

**Amendments to the Claims**

Please cancel Claims 18-59. The Claim Listing below will replace all prior versions of the claims in the application:

**Claim Listing**

- 1-59. (canceled)
60. (previously presented) A method of providing a clock to a synchronous memory comprising:
  - generating a driving clock signal with a delay locked loop (DLL);
  - buffering a clock input signal to provide a buffered clock signal;
  - providing the driving clock signal to a portion of the synchronous memory when the DLL is enabled; and
  - providing the buffered clock signal to said portion of the synchronous memory when the DLL is disabled.
61. (previously presented) The method of claim 60 further comprising providing register data to enable or disable the DLL.
62. (previously presented) The method of claim 60 further comprising providing a register bit to enable or disable the DLL.
63. (previously presented) The method of claim 60 further comprising providing a register to enable or disable the DLL.
64. (previously presented) The method of claim 60, wherein the DLL has an adjustable delay line and a delay comparator, the delay comparator determining the delay through the adjustable delay line.

65. (previously presented) The method of claim 64 further comprising the step of maintaining settings of the adjustable delay line when the DLL is disabled.
66. (previously presented) The method of claim 65 wherein the settings are maintained during power down.
67. (previously presented) The method of claim 65 wherein the settings are maintained during a standby state.
68. (previously presented) The method of claim 60 wherein said portion of the synchronous memory contains a data output buffer enabled by the driving clock signal or buffered clock signal.
69. (previously presented) A synchronous memory comprising:
  - means for generating a driving clock signal with a delay locked loop (DLL);
  - means for buffering a clock input signal to provide a buffered clock signal;
  - means for providing the driving clock signal to a portion of the synchronous memory when the DLL is enabled; and
  - means for providing the buffered clock signal to said portion of the synchronous memory when the DLL is disabled.